An 8 GHz MMIC PREAMPLIFIER*

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ABSTRACT

A monolithic GaAs low-noise 8 GHz preamplifier has been designed and fabricated on a 2.0 mm square chip. Measured gain, VSWR, and noise performance are described and compared to predicted values.

A monolithic GaAs low-noise amplifier covering the 7.25 to 7.75 and 7.75 to 8.25 GHz communications bands has been designed and fabricated using ion implantation technology. The 2.0 mm square chip contains input and output matching circuits with integrated DC blocking capacitors and on-chip bias networks including RF bypass capacitors. Measured gain, VSWR, and noise performance will be described and compared to computer predictions.

Circuit design considerations, in addition to performance, were minimization of chip size and incorporation of bias networks on-chip. Since bandwidth requirements were nominal for this amplifier, choice of simple 2-element tuning networks at input and output was consistent with the desire to minimize chip size and complexity. The choice of a series C-shunt L-matching topology gives access for biasing the gate and drain through the shunt indicators which are bypassed by large (>10 pF) on-chip MIM bypass capacitors.

The design procedure for this MMIC preamplifier began with a well-characterized equivalent circuit model for the 1 μm x 300 μm GaAs FET and proceeded according to the following steps.

1. Obtain FET noise parameters F_o, R_n, G_o, and B_o and FET S-parameters for desired band.

2. Choose topology, strive for minimum inductance and compatibility with on-chip biasing.

3. Design initial circuit with Smith chart, choose best compromise between noise figure and gain.

4. Perform complete circuit analysis for noise figure, gain, stability, and input and output matching. Optimize.

5. Do MMIC layout and estimate all parasitic elements.

6. Repeat steps 4 and 5 until design converges. Finalize layout.

The initial Smith chart analysis for noise and gain is shown in Figure 1. This figure shows constant noise figure circles and constant unilateral input gain circles at 8 GHz. A small source inductor was added to move the input match somewhat closer to the minimum noise tuning source impedance. The locus of the series C-shunt L-tuning network is shown from 6 to 10 GHz. It may be seen that this simple design tends to give both increased gain and increased noise as frequency is reduced due to the manner in which the design curves intersect. These curves are the starting point for the computer optimized final design.

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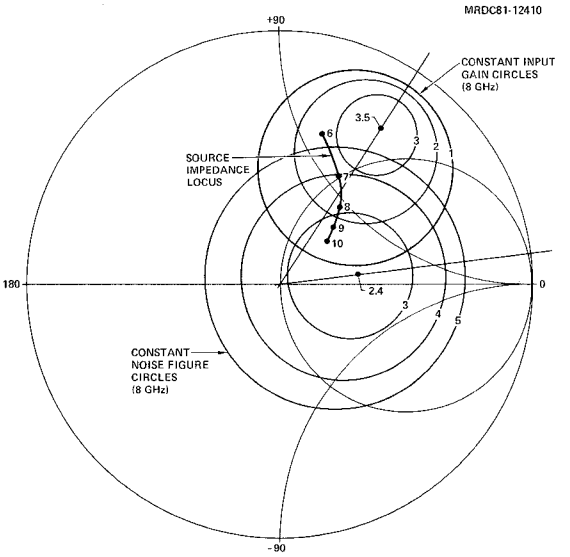

FIGURE 1: SMITH CHART ANALYSIS FOR NOISE AND GAIN

A schematic diagram of the preamplifier circuit is shown in Figure 2. The actual topology analyzed as extracted from the chip layout is considerably more complex than shown in the figure and includes bends, minor changes of line width, etc. Calculated amplifier performance is shown in Figure 3. Included in the computer model are the FET equivalent circuit, transmission line losses and dispersion effects, and the parasitic capacitances associated with the active and passive elements. However, the effects of loss are not included in the noise figure predictions. As shown in Figure 3, a gain of 7.0 dB with an associated noise figure of 3.0 dB is predicted for the preamplifier at 8 GHz.

The design is implemented as a microstrip circuit containing lumped and distributed matching elements on a semi-insulating (S.I.) GaAs substrate. Both Cr doped and undoped S.I. substrates grown by the horizontal Bridgman and the liquid encapsulated Czochralski (LEC) techniques have been used for device fabrication. A preselection test for bulk S.I. GaAs substrates involving qualification of the entire GaAs ingot by sampling the front and the rear of each boule is first employed to identify the ingot to be used. The qualification procedure assesses the ability of the S.I. substrate to withstand high temperature (850°C) processing and to yield device quality active layers by ion implantation. Direct, implantation of Si^+ in selected areas, defined photolithographically, is used for forming the FET and resistor active areas. The wafer is then coated with reactively sputtered Si_3N_4 and annealed at 850°C in a H_2 ambient resulting in active layers of ~1000 $\Omega/\square$ sheet resistivity and 4000-4500 $cm^2/V\text{-sec}$ Hall mobility at 1×10^{17} cm^{-3} doping concentration. AuGe/Ni is used to form the ohmic contacts. The 1 μm long gates are defined by conven-

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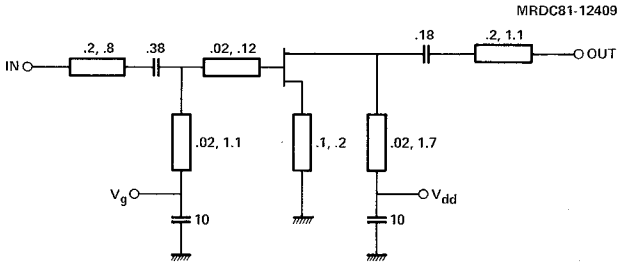

FIGURE 2: SCHEMATIC CIRCUIT DIAGRAM OF PREAMPLIFIER

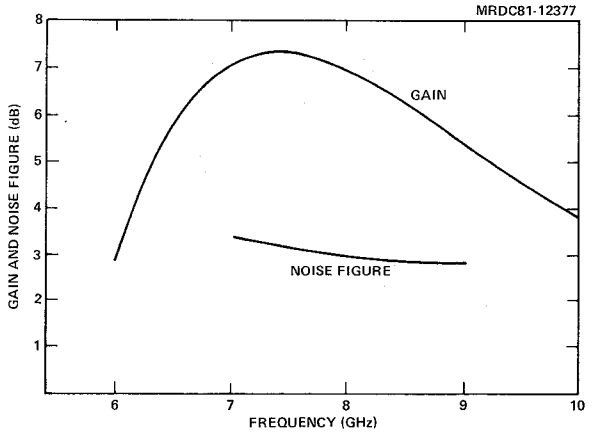

FIGURE 3: PREDICTED 8 GHz PREAMPLIFIER PERFORMANCE

tional photolithography and liftoff process.[1] Gate metal is Ti/Pt/Au for good reliability. A dielectric layer of Si_3N_4 is used for the insulator between the first level and second level interconnections and the dielectric for the circuit MIM capacitors. Typically, 130 pF/mm^2 capacitance is obtained. Capacitance uniformity and reproducibility can generally be maintained to within ±5%. Reactive ion etching is used to etch via holes in the dielectric wherever the first level metallization needs to be accessed. Second level metallization is formed by plating gold to a thickness of 2-3 μm to reduce RF losses in the passive circuitry. The GaAs substrate is thinned to 250 μm and back metallized to complete the ground plane of the microstrip transmission lines. Figure 4 is an SEM photograph of the complete circuit.

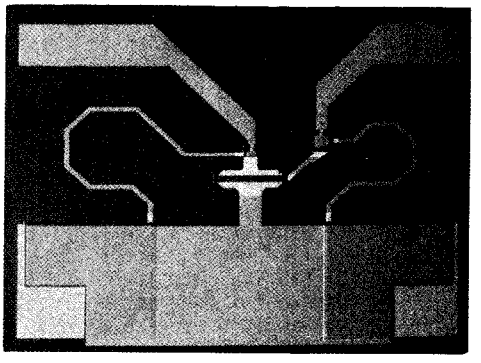

FIGURE 4: SCANNING ELECTRON MICROGRAPH OF 8 GHz MMIC AMPLIFIER CHIP

Figure 5 is a plot of the measured amplifier gain. The higher gain curve corresponds to a gate to source voltage of zero volts while the lower curve corresponds to the minimum noise bias of -1.3 volts. In each case, the drain to source voltage is 3.5 volts. Noise figures of 5.3, 5.5 and 4.2 dB were measured at 6.5, 7.5, and 8.5 GHz, respectively. Figure 6 shows the amplifier input and output match, which are both good over the band of interest. Agreement between predicted and measured gain is excellent. Noise figure is acceptable and is expected to be improved to the design value by further refinement of the circuit and FET.

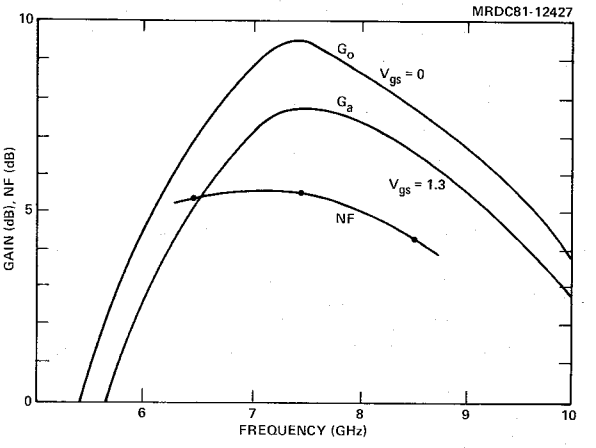

FIGURE 5: MEASURED PREAMPLIFIER GAIN AND NOISE FIGURE

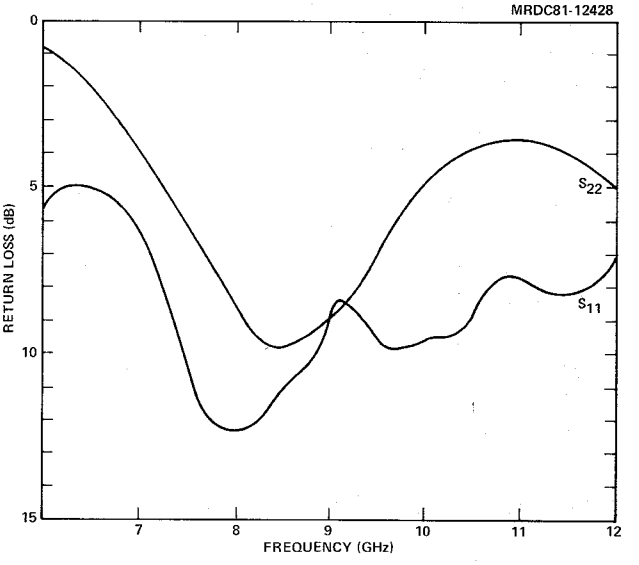

FIGURE 6: PREAMPLIFIER INPUT AND OUTPUT MATCH

References

1. A. K. Gupta, W. Petersen, "Monolithic GaAs Superheterodyne Front End," Interim Report No. 251-035/6-2-78, 427, Office of Naval Research, May 1980.